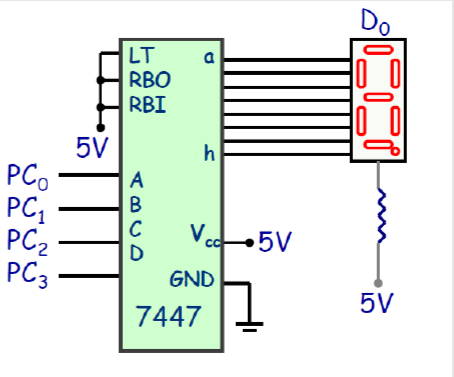
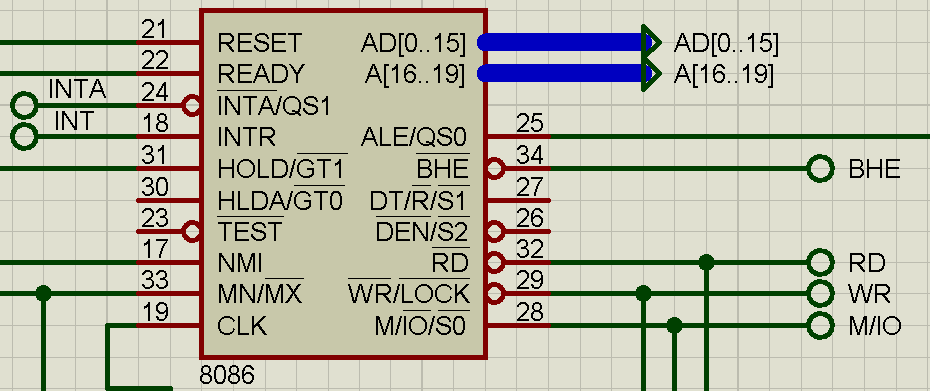
**7-SEGMENT DISPLAY**

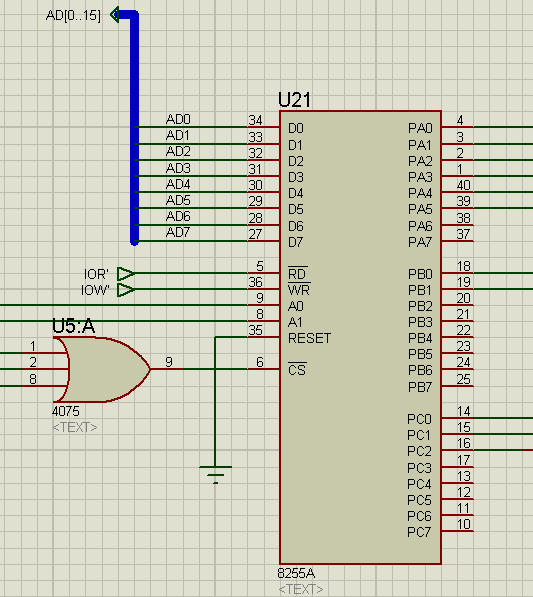


* 4 – seven segment displays showing the current floor of the elevator on each floor(including ground)
* 1 – seven segment display to show the destination floor where the elevator is moving
* Two 7447 are used.
* Each require 4 bits.

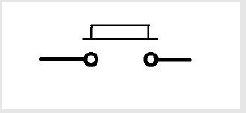
**8086 – INTEL MICROPROCESSOR**



**8255- INTEL Programmable Peripheral Interface chip**

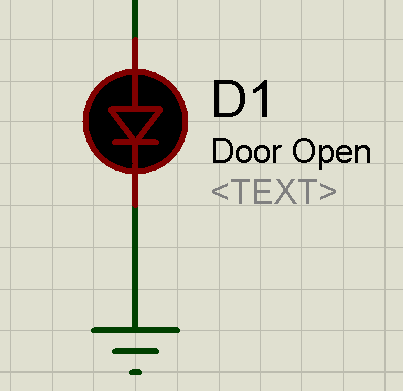


**PUSH BUTTON**

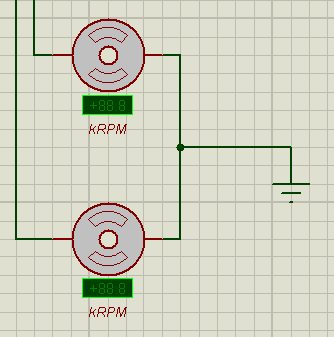


* Each coarse and fine sensor, floor button outside and inside the elevator have been assumed to be a push button pushed by the elevator as it moves.
* If not pressed, it generates a logic 0. This is being done to prevent the input from floating.

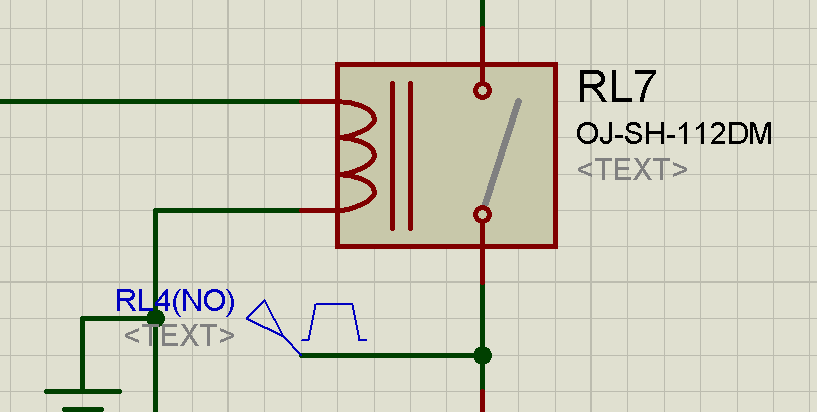
LED-LIGHT EMITTING DIODE



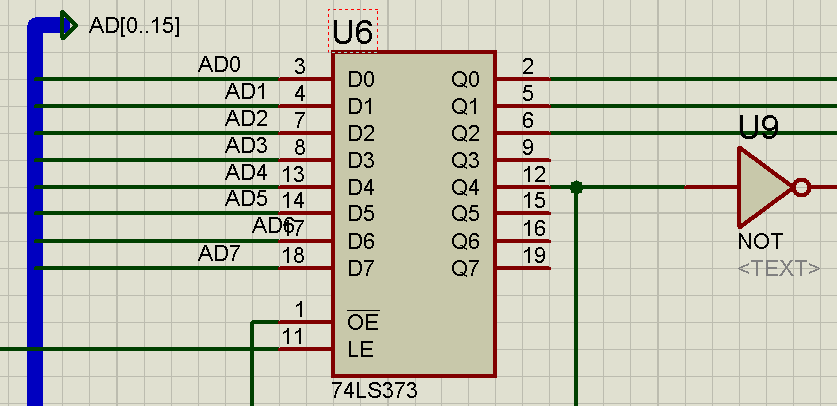
HEAVY DUTY SERVO MOTOR



RELAY



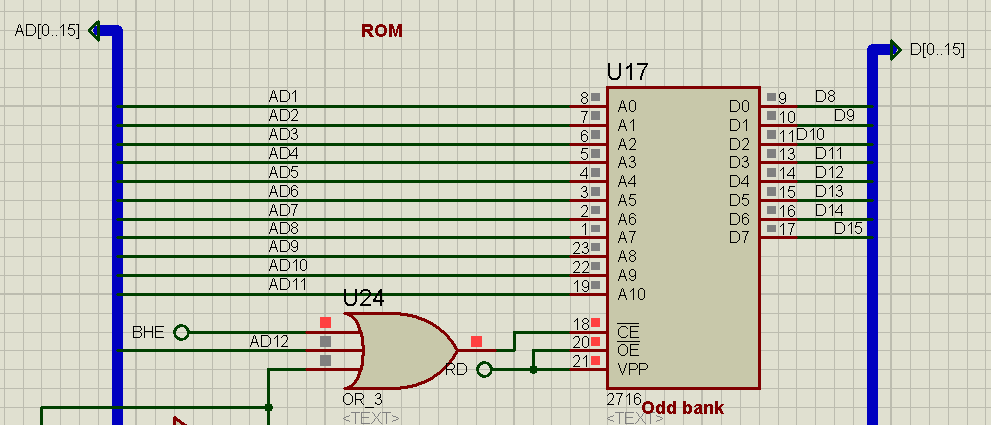
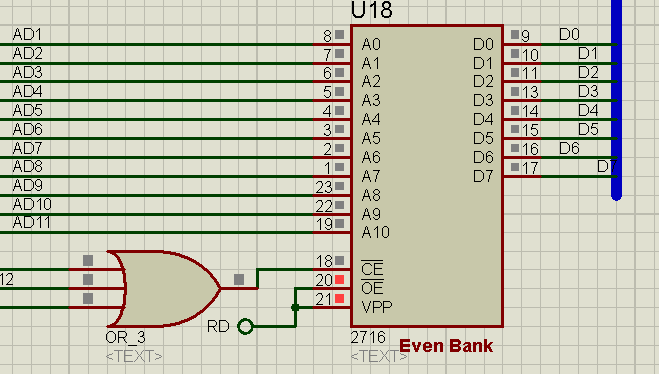
74LS373- OCTAL D-TYPE LATCH



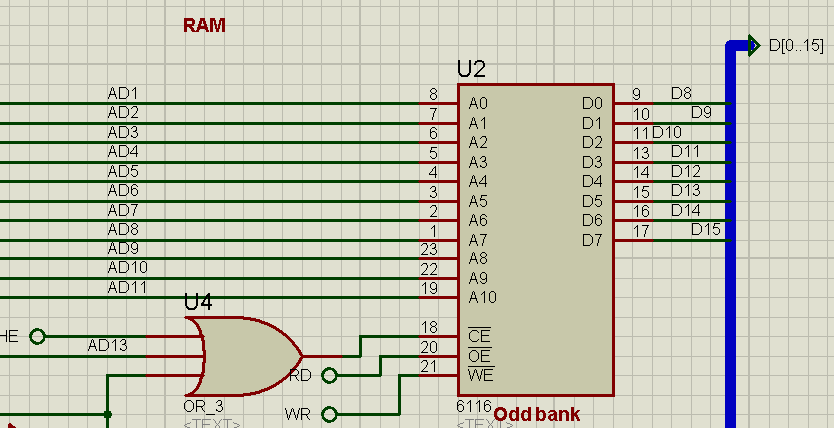
74LS343 consists of 8 latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

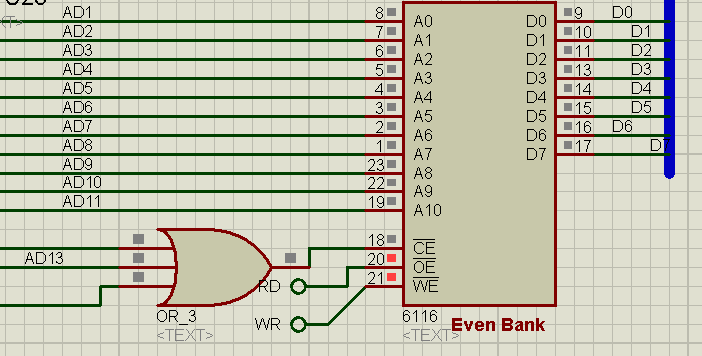
Two 74LS343 have been used in this design to de-multiplex the Address lines and interface the components in the system.

2716-(ROM-READ ONLY MEMORY)

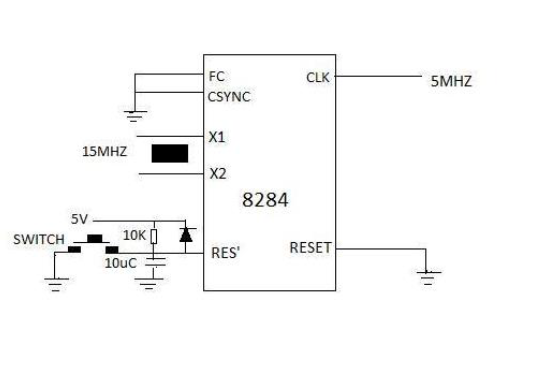


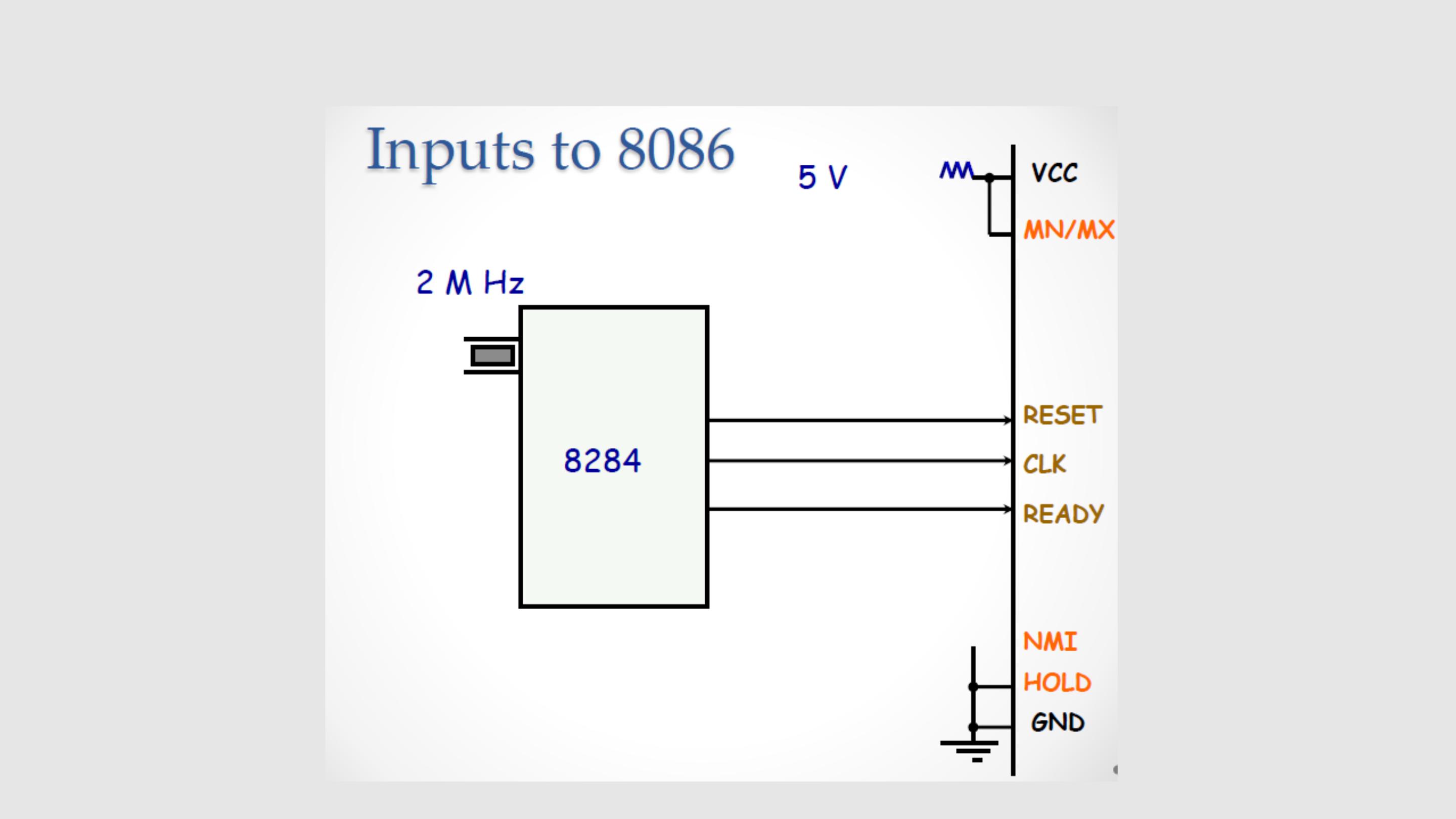
6116-(RAM-RANDOM ACCESS MEMORY)

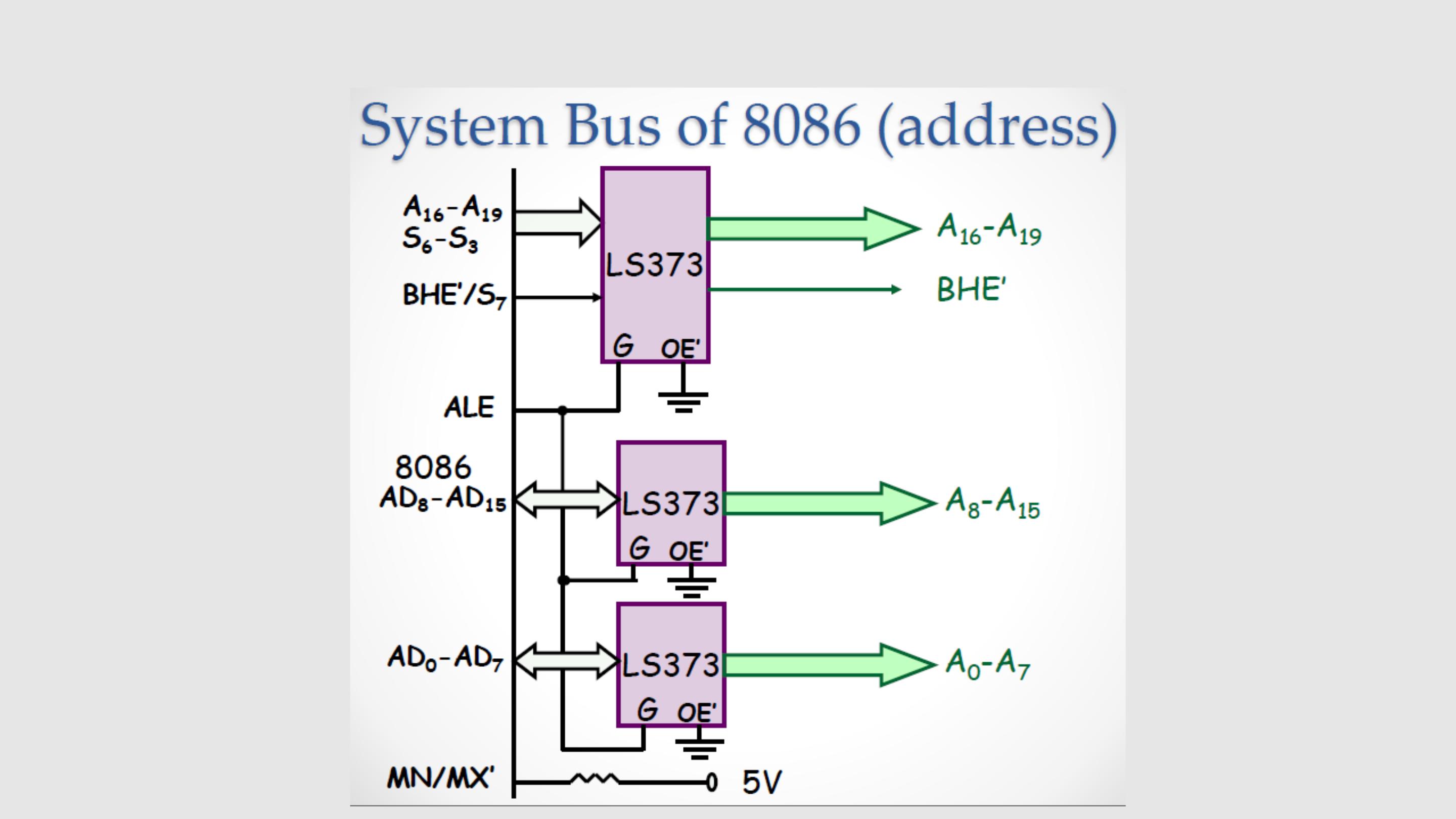




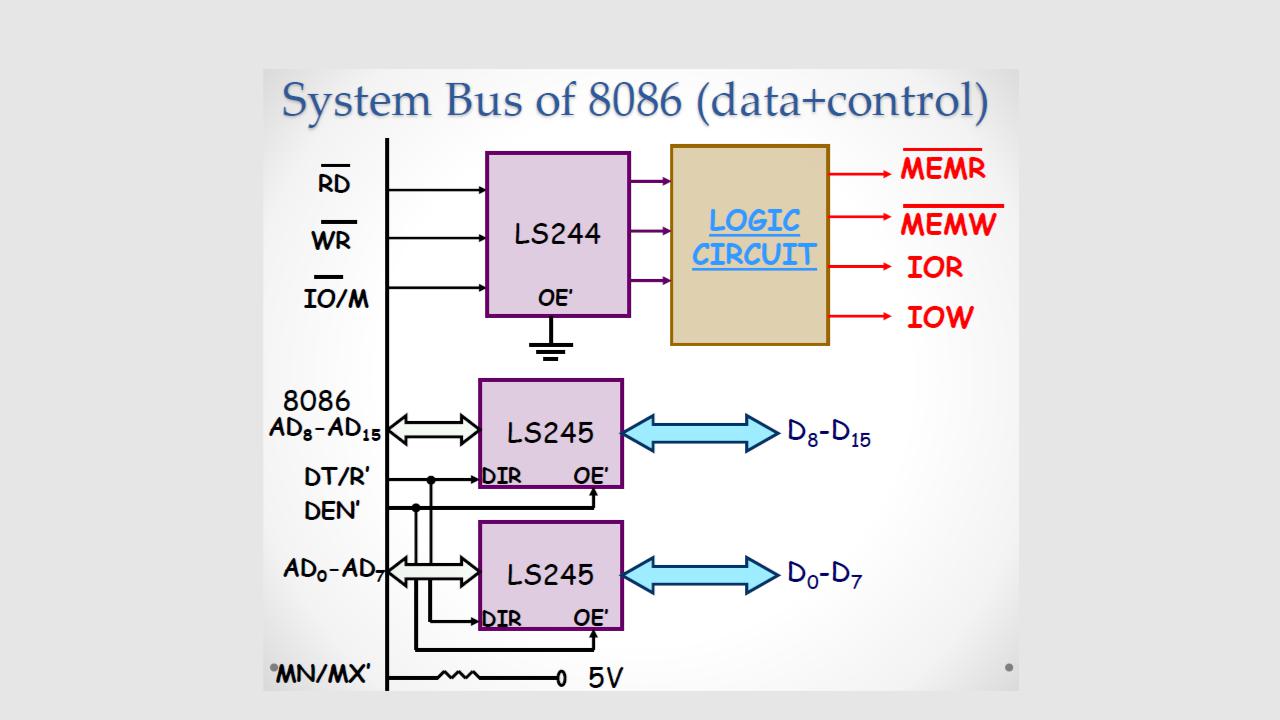
8284 CLOCK GENERATOR

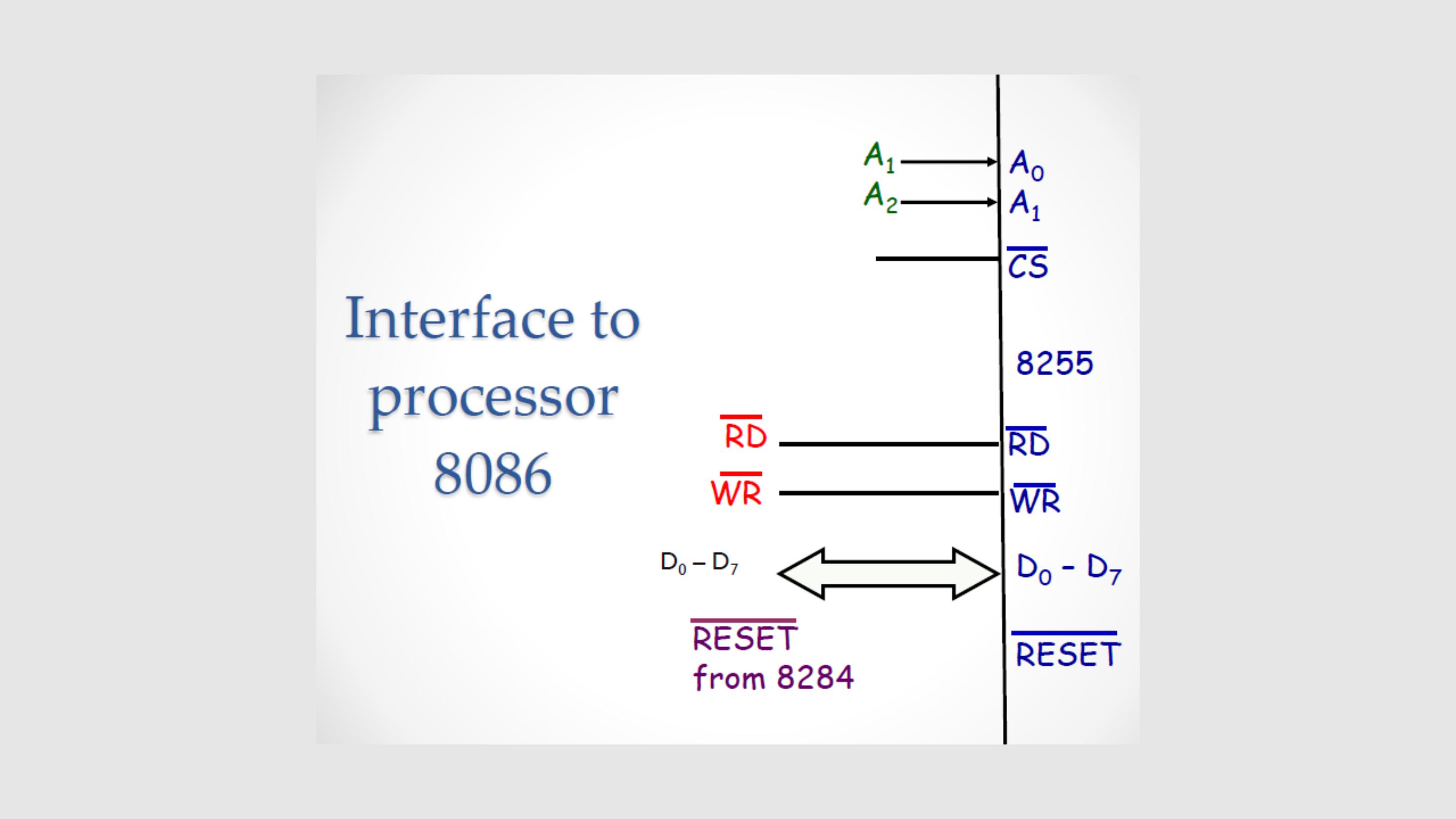


**Inputs to 8086**

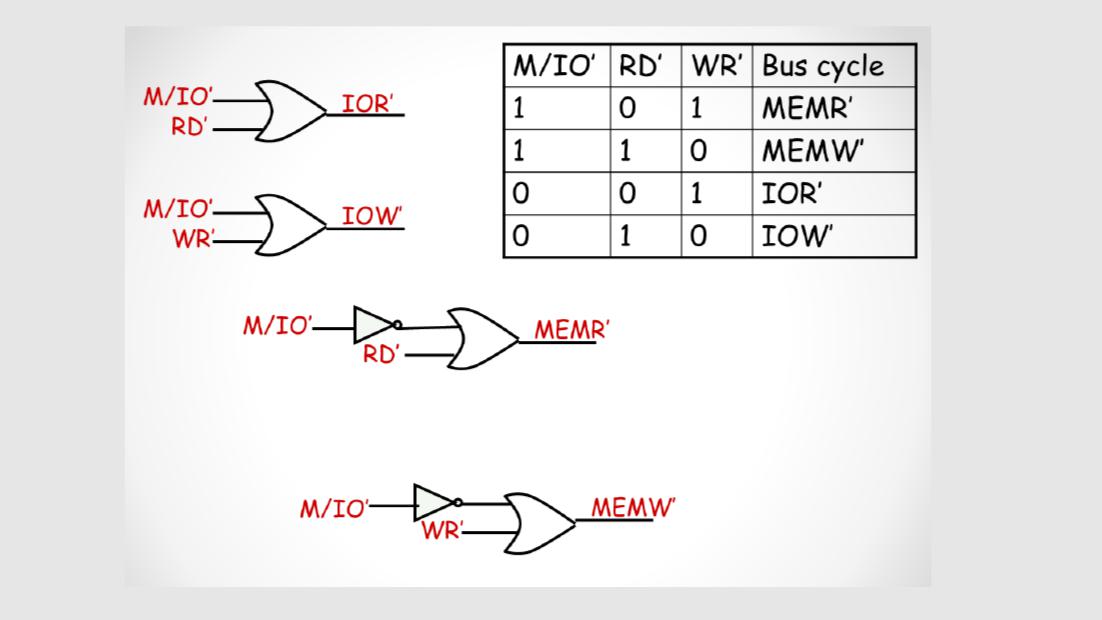


**System Bus of 8086(Address)**

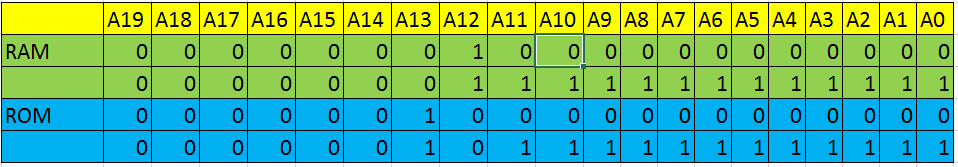
**System Bus of 8086(Data + Control)**



**Interface to processor 8086**



MEMORY MAPPING



RAMeven  01000H, 01002H, 01004H, …………. 01FFEH

RAModd 01001H, 01003H, 01005H, …………. 01FFFH

ROMeven 02000H, 02002H, 02004H, …………. 02FFEH

ROModd 02001H, 02003H, 02005H, …………. 02FFFH